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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/176,422	10/21/98	WILK G	TI-24742

EXAMINER	
BEREZNY, N	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 12/06/00

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/176,422	WILK ET AL.	
	Examiner	Art Unit	
	Neal Berezny	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 23-25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 1 and 18 are process claims and claims 23-25 are merely observed properties of material produced by the claimed process, and therefore does not serve to limit or alter the process itself. Observed properties of the product cannot be patented, only the process that makes the product can be patented in this case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro et al. (5,294,571) in combination with Nayar et al. (Electronic Letters, 2/1/90, vol.26, no.3). Fujishiro teaches forming a partially completed integrated circuit (IC), fig.2, el.1 and 9, where the substrate surface is cleaned, col.7, ln.8-12, and then exposed in an ozone ambient, col.4, ln.65-67, to form a gate oxide, el.6, and then forming a gate electrode over the gate oxide, el.7. Fujishiro fails to teach conducting the oxide growth

at a stable below 200 ^{0}C. Nayar anticipates growing an ultra-thin gate oxides, by UV formed ozone ambient, for microelectronic use, p.206, bottom of first col., after a surface cleaning. Nayar teaches using various stable temperatures, see fig.2, during exposure to an ozone ambient to obtain a thin high-grade oxide. It would be obvious to one of ordinary skill in the art to combine the teachings of Nayar with Fujishiro to form a low temperature gate oxide in Fujishiro's transistor by using stable temperatures, to form oxides of stable uniform thickness. Nayar provides the motivation to combine on page 205, col.1, start of paper, by pointing out the need to reduce the thermal budget, while maintaining control of the oxide growth rate, so as to avoid associated problems, such as wafer warpage and defect generation.

4. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro and Nayar as applied to claims 1-13 above, and further in view of Wolf, vol.3, p.422-423. Wolf teaches using a gate oxide in excess of 8 MV/cm, p.422, characteristic #4. It would be obvious to one of ordinary skill in the art to combine Wolf with Fujishiro and Nayar in order to reduce dielectric breakdown of the gate oxide to reduce catastrophic failure of the device.

5. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro and Nayar as applied to claim 18 above, and in view of Choquette et al. (5,275,687). In addition to the teaching described above Nayar also teaches the conversion of molecular oxygen to ozone with the use of UV light, see p.205, col.2, first

two chemical equations. Also taught by Nayar in the same equations is the use of an inert ambient in addition to the ozone. Further, Fujishiro also teaches keeping the ozone plasma not at the Si surface, col.5, ln.28-40.

6. Fujishiro and Nayar appear not to specifically state that the Si surface should be atomically flat. Choquette teaches a process to create an atomically flat or smooth surface prior to the formation of a high quality epitaxial layer, see abstract. It would be obvious to one of ordinary skill in the art to combine Choquette with Fujishiro and Nayar to form an atomically flat Si surface prior to the formation of a very thin gate oxide layer. One of ordinary skill in the art at the time of the invention would have been motivated to provide an atomically flat surface before forming a gate oxide that is only 2 or 3 atoms thick. Clearly a surface with deviations greater than 1 or 2 atoms thick would increase the likelihood of defects in the gate oxide resulting in an increase in the leakage current across the gate oxide layer.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro, Nayar, and Choquette as applied to claims 1-13 above, and further in view of Wolf, vol.3, p.422-423. Wolf teaches using a gate oxide in excess of 8 MV/cm, p.422, characteristic #4. It would be obvious to one of ordinary skill in the art to combine Wolf with Fujishiro, Nayar, and Choquette in order to reduce dielectric breakdown of the gate oxide to reduce catastrophic failure of the device.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro and Nayar as applied to claim 18 above, and in view of Cook et al. (5,194,397). Fujishiro and Nayar appear not to specifically state that the cleaned surface, prior to oxidation, be hydrogen terminated. Cook teaches the art of hydrogen terminating an exposed Si surface, col.3, ln.39-49. It would be obvious to one of ordinary skill in the art to combine Cook with Fujishiro and Nayar to hydrogen terminate the Si surface in order to passivate the surface to keep it clean and prevent unwanted or uncontrolled reaction with the silicon surface. This would help reduce defect densities in the subsequently formed gate oxide.

9. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro and Nayar as applied to claim 18 above, and in view of Faraone et al. (4,604,304) and Doklan et al. (4,851,370). Fujishiro and Nayar do not specifically teach the use of multiple layers of oxide for a thicker gate oxide layer. Faraone teaches forming a silicon layer on the first oxide and then oxidizing it for a thicker oxide, col.4, ln.39-42. It would be obvious to one of ordinary skill in the art to combine Faraone with Fujishiro and Nayar, to form a thicker two-layer gate oxide. Doklan teaches forming two oxide layers on top of each other to misalign the defects of each layer in order to reduce leakage current, thereby providing the motivation to combine Faraone and Doklan with Fujishiro and Nayar.

10. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro, Nayar, and Choquette as applied to claims 1-13 above, and further in view of Faraone et al. (4,604,304) and Doklan et al. (4,851,370). Fujishiro and Nayar do not specifically teach the use of multiple layers of oxide for a thicker gate oxide layer. Faraone teaches forming a silicon layer on the first oxide and then oxidizing it for a thicker oxide, col.4, ln.39-42. It would be obvious to one of ordinary skill in the art to combine Faraone with Fujishiro, Nayar, and Choquette, to form a thicker two-layer gate oxide. Doklan teaches forming two oxide layers on top of each other to misalign the defects of each layer in order to reduce leakage current, thereby providing the motivation to combine Faraone and Doklan with Fujishiro, Nayar, and Choquette.

Response to Arguments

11. Applicant's arguments filed 9/26/00 have been fully considered but they are not persuasive. Applicant argues that claim 18 is patentable because claim 18 contains a limitation that the gate oxide layer be uniformly thick. It is well-known in the art to form gate oxides that are uniformly thick, as taught in Wolf, vol.3, page 422, characteristic #2, and would be obvious to one skilled in the art in order to reduce dielectric failure of the device.

12. Applicant alleges a highly uniform gate oxide and superior properties as demonstrated in fig.3 of the specifications. Patentability of a process cannot be based solely on the mere allegation of a superior product. The process must be shown to be novel and non-obvious, which applicant has not done in their response.

13. Applicant also challenges the reference Choquette, as not teaching an atomically flat silicon surface. Applicant's attention is drawn to the bottom of the abstract for Choquette.

CONCLUSION

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on Monday to Friday from 7:00 to 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached at (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

WAEL FAHMY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

12-4-00

Neal Berezny

Patent Examiner

Art Unit 2823